CLAIMS

What is claimed is:

1. A bus system for transferring signals from a plurality of signal streams to an output, the bus system comprising:

a plurality of signal buses in parallel; and

a control system for multiplexing the signals from two or more of the plurality of signal streams onto two or more of the plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses before demultiplexing the signals to the output.

2. The bus system as set forth in claim 1 wherein the control system provides binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

3. The bus system as set forth in claim 1 wherein the control system provides interpolation by coupling each of the signals from each of the plurality of signal buses to the output separately and each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time.

4. The bus system as set forth in claim 1 wherein one of the plurality of signal buses is coupled to each of the plurality of signal streams.

5. The bus system as set forth in claim 1 wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.

6. The bus system as set forth in claim 1 wherein the control system comprises:

a decoder;

a first control circuit coupled to the decoder; and

a plurality of first switches coupled to the first control circuit, each of the plurality of first switches also being coupled between one of the plurality of signal streams and one of the plurality of signal buses.

7. The bus system as set forth in claim 6 wherein the decoder is a sequential decoder.

8. The bus system as set forth in claim 6 wherein the decoder is a random decoder.

9. The bus system as set forth in claim 6 wherein the control system further comprises:

an address counter coupled to the decoder;

a second control circuit coupled to the address counter; and

a plurality of second switches coupled to the second control circuit, each of the plurality of second switches also being coupled between one of the plurality of signal buses and the output.

10. An imager comprising:

a plurality of streams of signals from a source;

a plurality of signal buses in parallel;

an output; and

a control system for multiplexing the signals from two or more of the plurality of signal streams onto two or more of the plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses before demultiplexing the signals to the output.

11. The imager as set forth in claim 10 wherein the control system provides binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

12. The imager as set forth in claim 10 wherein the control system provides interpolation by coupling each of the signals from each of the plurality of signal buses to the output separately and each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time.

13. The imager as set forth in claim 10 wherein one of the plurality of signal buses is coupled to each of the plurality of signal streams.

14. The imager as set forth in claim 10 wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.

15. The imager as set forth in claim 10 wherein the control system comprises:

a decoder;

a first control circuit coupled to the decoder; and

a plurality of first switches coupled to the first control circuit, each of the plurality of first switches also being coupled between one of the plurality of signal streams and one of the plurality of signal buses.

16. The imager as set forth in claim 15 wherein the decoder is a sequential decoder.

17. The imager as set forth in claim 15 wherein the decoder is a random decoder.

18. The imager as set forth in claim 15 wherein the control system further comprises:

an address counter coupled to the decoder;

a second control circuit coupled to the address counter; and

a plurality of second switches coupled to the second control circuit, each of the plurality of second switches also being coupled between one of the plurality of signal buses and the output.

19. The imager as set forth in claim 10 further comprising a video processing circuit coupled to the output.

20. The imager as set forth in claim 19 wherein the video processing circuit provides differential processing.

21. A bus system for transferring signals from a plurality of signal streams to an output, the bus system comprising:

a plurality of signal buses coupled to the plurality signal streams;

a plurality of first switches, each of the plurality of first switches coupled between one of the plurality of signal streams and one of the plurality of signal buses;

a plurality of second switches, each of the plurality of second switches coupled between one of the plurality of signal buses and the output; and

a control system coupled to the first and second switches, the control system closing two or more of the plurality of first switches to couple signals from the two or more of the plurality of signal streams to two or more of the plurality of signal buses and allowing the signals to substantially charge each of the two or more of the plurality of signal buses before closing one or more of the plurality of second switches to couple the signals to the output.

22. The bus system as set forth in claim 21 wherein the control system provides binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.

23. The bus system as set forth in claim 21 wherein the control system provides interpolation by coupling each of the signals from each of the plurality of signal buses to the output separately and each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time.

24. The bus system as set forth in claim 21 wherein one of the plurality of signal buses is coupled to each of the plurality of signal streams.

25. The bus system as set forth in claim 21 wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.

26. The bus system as set forth in claim 21 wherein the control system comprises:

a decoder;

a first control circuit coupled to the decoder and the plurality of first switches

an address counter coupled to the decoder; and

a second control circuit coupled to the address counter and to the plurality of second switches.

27. The bus system as set forth in claim 26 wherein the decoder is a sequential decoder.

28. The bus system as set forth in claim 26 wherein the decoder is a random access decoder.

29. A method for transferring signals comprising:

multiplexing signals on to two or more of a plurality of signal buses; and

allowing the signals to substantially charge each of the two or more of the plurality of signal buses before demultiplexing the signals to an output.

30. The method as set forth in claim 29 further comprising binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together.